Analysis and Simulation of Gate Leakage Current in P3 SRAM Cell at Deep-Sub-Micron Technology for Multimedia Applications

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***Abstract*—In this paper the gate leakage current analysis of the Conventional 6T SRAM, NC-SRAM, PP SRAM, and P3 SRAM cell has been carried out. It has been observed that due to pMOS stacking and direct supply body biasing in the P3 SRAM Cell, there is a reduction of gate leakage current 66.55%, 34.42%, and 90.99% with respect to the 6T, NC-Cell, and PP cell, respectively for V_{DD}=0.8V. For V_{DD}=0.7V, it is found 82.2%, 75.35%, and 93.15%, respectively. The total standby leakage power in P3 SRAM Cell is found significantly reduced by 69.07%, 13.61%, and 81.01% at V_{DD}=0.8V and 73.07%, 16.79%, and 87.94% at V_{DD}=0.7V, with respect to the Conventional 6T SRAM Cell, NC-SRAM Cell, and PP SRAM Cell. The simulation is being performed at t_{ox} =2.4nm, V_{DD} = 0.8V and 0.7V, V_{thn}=0.22V, and V_{thp}=0.224V.**

***Index Terms*—CONVENTIONAL 6T SRAM BIT CELL, PP-SRAM, NC-SRAM, P3-SRAM, GATE TUNNELING LEAKAGE CURRENT, STACKING.**

I. Introduction

Portable multimedia is growing at a startling rate. This is fueling the trend toward rich multimedia and communications capabilities on portable devices. End users in the handheld wireless market segment are demanding multimedia and communication experiences similar to those they enjoy on their desktop-but in a mobile setting. Video playback, Multi-player gaming, and Video conferencing, High speed Internet are a few of the key applications driving the path to higher performance multimedia. One of the biggest challenges for multimedia on portable devices is to provide high performance with low power consumption. In other words, it demands the processor with high processing power, high performance, and low-power on-chip memory. According to the ITRS-2003 (International Technology Roadmap), 90% of the chip-area will be occupied by the memory core by 2014 [1]. This shows the more demand for chips with high functionality and low-power consumption. So to achieve Low-power SRAM cell, it is important to focus on minimizing the Leakage power of the SRAM structures, which is directly connected to the different Leakage currents in the Cell. There are several sources for the Leakage current, i.e. the Sub-threshold current due to low threshold voltage, the Gate Leakage current due to very thin gate oxides, etc., [2]. In this work, a P3 SRAM cell structure designed for reduction of Leakage power in both active and standby mode through the Gate Leakage current reduction is analyzed. Our main focus is Static power dissipation and the Gate Leakage model of the Cell in the standby mode. The rest of the paper is organized as follows, in section II a brief review of conventional 6T SRAM bit-cell is included and basic of leakage current mechanisms is presented in section III. The section IV reviews the PP, NC and the P3 SRAM designs followed by analysis of the Gate Leakage model of P3 SRAM cell in section V. The simulation results and conclusions are discussed in section VI and VII respectively.

II. Conventional 6T Sram Bit-Cell

The conventional SRAM (CV-SRAM) cell has six MOS transistors (4 nMOS and 2 pMOS), Fig 1. Unlike DRAM it doesn't need to be refreshed as the bit is latched in. It can operate at lower supply voltages and has large noise immunity. However, the six transistors of an SRAM cell take more space than a DRAM cell made of only 1 transistor and 1 capacitor, thereby increasing the complexity of the cell [3].

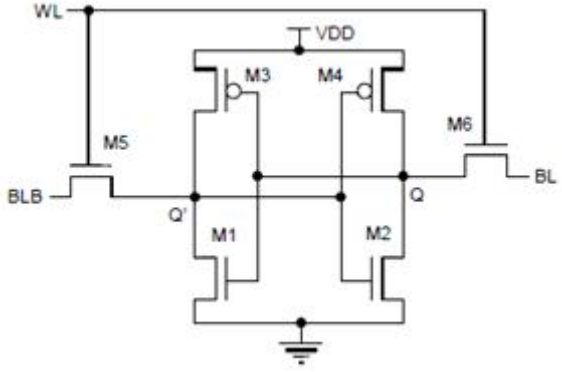

Figure 1. 6T SRAM Bit-cell

The memory bit-cell has two CMOS inverters connected back to back (M1, M3, and M2, M4). Two more pass transistors (M5 and M6) are the access transistors controlled by the Word Line (WL), Fig.1. The cell preserves its one of two possible states "0" or "1", as long as power is available to the bit-cell. Here, Static power dissipation is very small. Thus the cell draws current from the power supply only during switching. But idle mode of the memory is becoming the main concern in the deep–sub-micron (DSM) technology due to its concerns in the leakage power and data retention at lower

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operating voltages. Although the two nMOS and pMOS transistors of SRAM memory bit-cell form a bi-stable latch, there are mainly three states of SRAM memory cell the Write, Read, and Hold states [4].

III. Leakage Current Mechanisms

High leakage current in deep-submicron regimes is the major contributor of power dissipation of CMOS circuits as the device is being scaled. Various leakage mechanisms are show in Figure 2 [5].

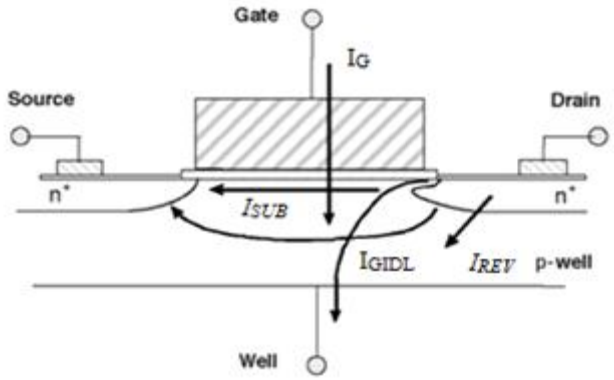

Figure 2. Leakage current mechanisms of deep-submicron transistors

A. Gate Direct Tunneling Leakage (I_G)

The gate leakage flows from the gate through the "leaky" oxide insulation to the substrate. In oxide layers thicker than 3–4nm, this kind of current results from the Fowler-Nordheim tunneling of electrons into the conduction band of the oxide layer under a high applied electric field across the oxide layer. For lower oxide thicknesses (which are typically found in 0.15µm and lower technology nodes), however, direct tunneling through the silicon oxide layer is the leading effect. Mechanisms for direct tunneling include electron tunneling in the conduction band (ECB), electron tunneling in the valence band (EVB), and hole tunneling in the valence band (HVB), among which ECB is the dominant one. The magnitude of the gate direct tunneling current increases exponentially with the gate oxide thickness t_{ox} and supply voltage V_{DD}. In fact, for relatively thin oxide (in the order of 2-3 nm), at a VGS of 1V, every 0.2nm reduction in t_{ox} causes a tenfold increase in I_G [2]. Gate leakage increases with temperature at about 2x/100ºC.

The gate tunneling current components include the tunneling current between gate and substrate (Igb), and the current between gate and channel (Igc), which is partitioned between the source and drain terminals by Igc = Igcs + Igcd. The third component happens between gate and source/drain diffusion regions (Igs and Igd). Figure 3 shows the schematic gate tunneling current flows.

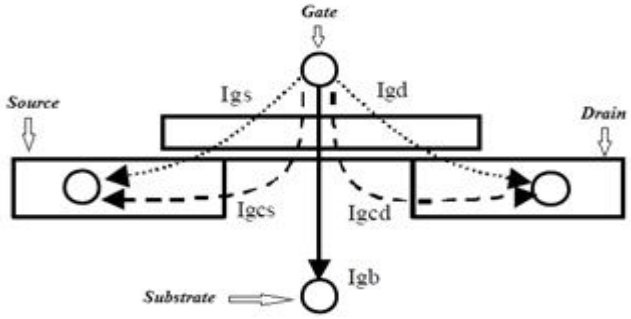

Figure 3. Leakage current mechanisms of deep-submicron transistors

B. Sub-threshold leakage (I_{SUB})

The Sub-threshold Leakage Current is the drain-to-source leakage current when the transistor is in the OFF mode. This happens when the applied voltage VGS is less than the threshold voltage V_T of the transistor, i.e., weak inversion mode. Sub-threshold current flows due to the diffusion current of the minority carriers in the channel of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Equation (1) relates sub-threshold power ISUB with other device parameters.

$$P_{Sub-Vf} = \frac{\mu W_{eff}}{L_{eff}} C_{ox}.V_T{}^2.e^{(|V_{GS}|-V_T)/\eta V_T}.(1-e^{-|V_{DS}|/V_T}) \quad (1)$$

Where, $V_T = \frac{KT}{q}$

P_{Sub-Vf} - Sub-threshold Power, W_{eff}– channel effective width, L_{eff} – channel effective length, V_{DS}- Drain-Source Voltage, µ-Mobility, C_{ox}– Oxide capacitance, V_T- Thermal voltage, V_{GS}-Gate-Source Voltage, K- Boltzmann's Constant, T-Temperature, q– Charge.

As the supply voltage (V_{DD}) is being uniformly scaled down with successive technology nodes. The transistor delay is inversely proportional to the difference of supply and threshold voltage [6], the threshold voltage must also be scaled down proportionally with each technology node to maintain the circuit performance. This leads to an exponential increase in sub-threshold leakage current. Also, increasing the threshold voltage (V_T) of the transistor is an effective way to reduce sub-threshold leakage.

C. Reverse-Biased Junction Leakage (I_{REV})

The junction leakage occurs from the source or drain to the substrate through the reverse biased diodes when a transistor is in the OFF mode. A reverse-biased pn junction leakage has two main components, one is due to the minority carrier diffusion/drift near the edge of the depletion region and the other is due to electron-hole pair generation in the depletion region of the reverse-biased junction. For Ex: in a CMOS inverter with low input voltage, the nMOS is OFF, the pMOS is ON and the output voltage is high. Subsequently, the drain-to-substrate voltage of the OFF nMOS transistor is equal to the supply voltage (V_{DD}). This results in a leakage

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current from the drain to the substrate through the reverse-biased diode. If both n and p regions are heavily doped, Band-to-Band Tunneling (BTBT) dominates the pn junction leakage [7]. The junction leakage has a rather high temperature dependency (i.e., around 50–100x/100 °C).

D. Gate-Induced Drain Leakage (I_{GIDL})

The Gate Induced Drain Leakage (GIDL) is caused by high field effect in the drain junction of MOS transistors. In an nMOS transistor with grounded gate and drain potential at V_{DD}, the significant band bending in the drain allows the electron-hole pair generation through avalanche multiplication and band-to-band tunneling. A deep depletion condition is created since the holes are rapidly swept out to the substrate. At the same time, electrons are collected by the drain, resulting in GIDL current. This leakage mechanism is made worse by high drain to body voltage and high drain to gate voltage. Thinner oxide and higher supply voltage increase GIDL current. For Ex: with a V_{DG}=3V and t_{ox} = 4nm, there is roughly a 10 fold increase in the GIDL current when V_{DB} is increased from 0.8V to 2.2V.

IV. A Review Of Related Work

In this section, we have reviewed some of the previously proposed SRAM cells. The NC SRAM [8] cell uses dual-threshold voltage process technology. In NC SRAM high V_t transistors are used in certain key leakage prone parts of the cell. In addition it uses Supply Voltage Gating to achieve Leakage saving.

The NC SRAM cell uses two transistors NC1, NC2 that provide different ground supply voltage to memory cell for normal and sleep modes. The pass transistor provides a positive ground supply voltage when the cell is inactive and connect the cross coupled inverters to the ground during normal operation to function as a conventional 6T-cell.

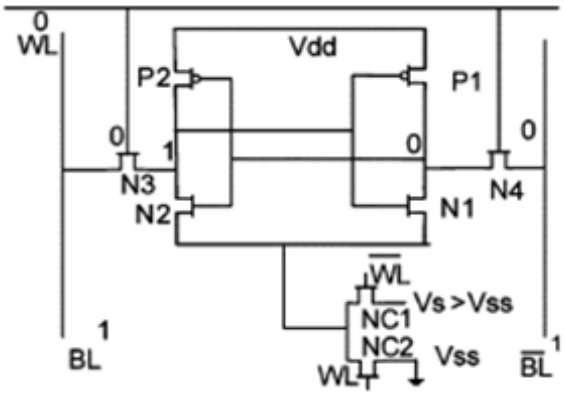

Figure 4. The NC SRAM Bit-cell [7]

In [9], a Gate Leakage current reduction technique based on the pMOS pass-transistor SRAM bit-cell structure as PP-SRAM cell has been proposed at 45nm technology and 0.8V supply voltage. In this cell, in order to decrease the gate leakage currents of the SRAM bit cell, nMOS pass transistors are replaced by pMOS pass transistors. The use of pMOS leads to performance degradation due to different mobility coefficients for the nMOS and pMOS transistors. To overcome this problem, the width of pMOS pass transistor is selected as 1.8 times of that of the nMOS for technology used in this work. Thus, has area penalty.

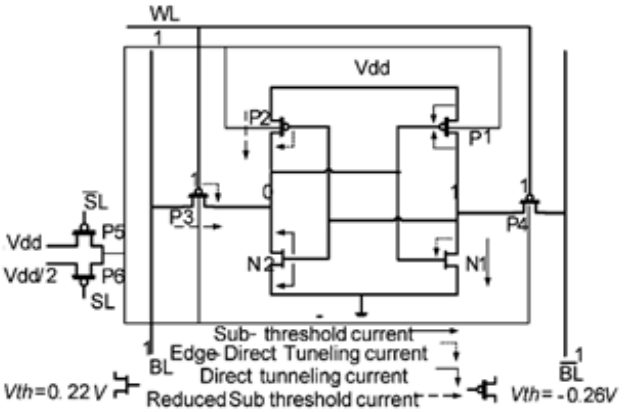

Figure 5. PP SRAM with Gate Leakage Currents [8]

In [3], a P3 SRAM bit-cell structure at 45nm technology has been proposed for semiconductor memories with high activity factor based applications in deep sub-micron CMOS technology. The cell has been proposed for the reduction of leakage power through the gate leakage current and sub-threshold leakage current reduction in both active and standby mode of the memory operation. The stacking transistor pMOS, connected in series (in line), is kept off in standby mode and kept on in active (read/write) mode. The pMOS transistors are used to lower the gate leakage current [9] while full-supply body-biasing scheme is used to reduce the sub-threshold leakage currents. P3 SRAM bit-cell made a significant fall in dynamic as well as standby powers in comparison to the conventional 6T SRAM bit cell, at the cost of small area penalty and issues with SNM.

V. Gate Leakage Current Analysis In P3-Sram Bit-Cell

In this section we proposed the Gate Leakage Model of the P3-SRAM cell. In [3], the P3 SRAM Bit–Cell structure has been proposed, in order to decrease the Gate Leakage current in the P3 cell the nMOS pass transistors have been replaced by the pMOS pass transistors PM2 and PM3. In the standby mode WORD LINE (WL) is charged to '1' to turn off the two pass transistors PM2 and PM3, so the cell is cut off from BL and BLB. In the mean time BIT LINES are charged to '1'. Now the Gate Leakage component for the pass transistor PM2 and PM3 is only I_{GD3}, the pass transistor PM3 has no Gate Leakage component. While in conventional 6T SRAM the Gate Leakage components for the pass transistors are I_{GD2}, I_{GD3}, I_{GS4} [9]. A pMOS transistor has also been introduced between the cell and the ground, hence utilizing the concept of stacking [10]. However the introduction of the stacking transistor PM4 introduces a voltage greater than zero at the source terminals of NM0 and NM1 transistors. Due to the introduction of positive voltage at the source terminal an extra Gate Leakage component I_{GS0} is introduced which is neutralized by the reduction in the Gate Leakage (I_{GS1}) of transistor NM1.

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In the Standby mode the transistor PM4 is in OFF state, so it acts as a barrier between the Leakage current of the BIT-CELL and the GND. As all the Leakage current has to pass to ground through PM4, so further in the standby mode it greatly reduces the Gate Leakage current.

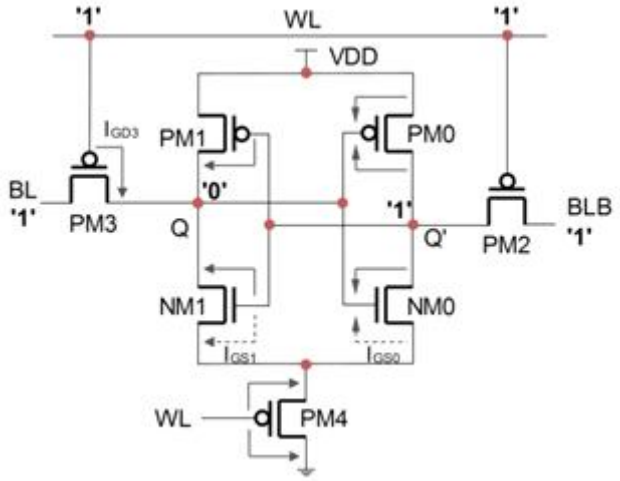

Figure 6. The P3 SRAM Bit-cell

VI. Results And Discussion

A.. Gate leakage current (I_G)

To analyze the Gate leakage currents and standby power in the 6T, PP, NC and P3 SRAM Cells, the simulation work is being performed in Cadence Virtuoso Schematic for 45nm technology with oxide thickness of 2.4nm at 27°C and the supply voltage of V_{DD}=0.8V and 0.7V are used.

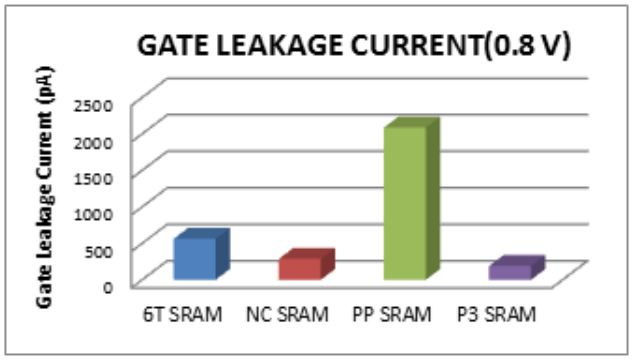

Figure 7. Gate Leakage Comparison at 0.8V

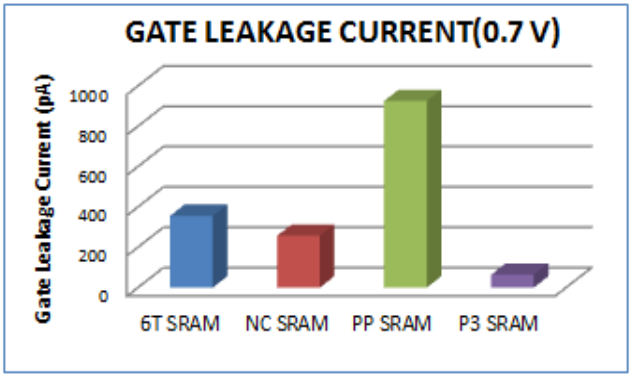

Figure 8. Gate Leakage Comparison at 0.7V

Fig. 7 and 8 shows the comparison of Gate leakage current in standby mode for 6T, NC, PP and P3 SRAM Bit cell. There is a significant reduction of gate leakage current in P3 SRAM due to use of pMOS pass transistors, use of gated pMOS and direct supply body biasing. There is a reduction of Gate Leakage current 66.55%, 34.42%, and 90.99% for V_{DD}=0.8V and 82.2%, 75.35%, and 93.15%, for V_{DD}=0.7V with respect to the 6T, NC-Cell, and PP cell respectively.

B. Static power consumption

Fig. 9 shows the total standby power consumption of all the four designs. It is evident from the simulation results that due to the lowering of the Gate Leakage current in the P3 SRAM, the reduction in total standby power of up to 74.1% has been achieved as compared to 6T SRAM Bit Cell.

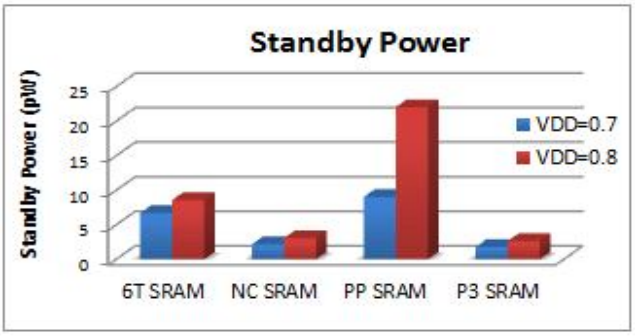

Figure 9. Standby Power Comparison

C. Area

Fig. 10 shows a relative comparison of the bit-cell area of the four SRAM designs. It is evident that the cell area is largest in case of P3 SRAM, however, as the gated transistor is of minimum feature size, so the area penalty is minimum in terms of a large memory.

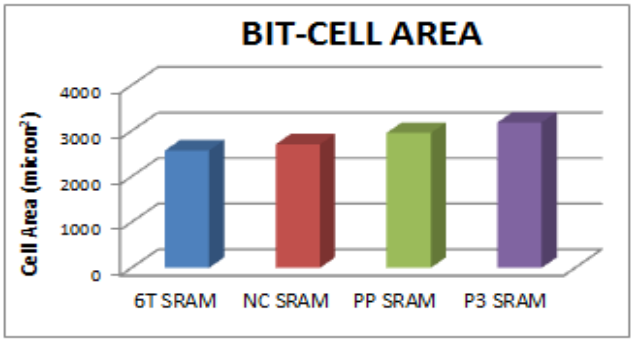

Figure 10. Bit Cell Area

Conclusion

In this paper the Gate Leakage current analysis of the for the Conventional 6T SRAM , NC-SRAM, PP SRAM, and P3 SRAM cell has been carried out. It has been observed that due to pMOS stacking and direct supply body biasing in the P3 SRAM Cell, there is a reduction of gate leakage current 66.55%, 34.42%, and 90.99% with respect to the 6T, NC-Cell, and PP cell, respectively for V_{DD}=0.8V and for V_{DD}=0.7V, it is found 82.2%, 75.35%, and 93.15%, respectively. The total standby leakage power in P3 SRAM Cell is found significantly

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reduced by 69.07%, 13.61%, and 81.01% at V_{DD}=0.8V and 73.07%, 16.79%, and 87.94% at V_{DD}=0.7V, with respect to the Conventional 6T SRAM Cell, NC-SRAM Cell, and PP SRAM Cell. The area penalty is 1.2%, 1.1%, and 1%, with respect to the 6T Cell, NC-SRAM, and PP Cell, respectively.

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